AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of designing a memory system for implementation using an integrated circuit, comprising:

receiving specification data including attributes of said memory system;

~~generating a logical description of said memory system in response to said specification data, said logical description defining a memory component and a memory interconnection component; and~~

configuring a memory component and a memory interconnection component of a memory model in response to the specification data to generate a logical view of said memory system; and

generating a physical description of said memory system in response to said logical ~~description~~ view, said physical description including memory circuitry associated with said integrated circuit defined by said memory component, said memory circuitry having an interconnection topology defined by said memory interconnection component.

2. (Original) The method of claim 1, further comprising:

defining said specification data using a set of primitives configured to generate descriptions for said memory system attributes.

3. (Original) The method of claim 2, wherein said set of primitives comprises extensible markup language (XML) constructs.

4. (Original) The method of claim 1, wherein said memory circuitry is disposed within said integrated circuit.

5. (Original) The method of claim 1, wherein a portion of said memory circuitry is disposed within said integrated circuit, and a remaining portion of said memory circuitry is disposed external to said integrated circuit.

6. (Original) The method of claim 1, wherein said memory component is defined by a memory architecture and a memory interface, and wherein said memory-interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface.

7. (Original) The method of claim 6, wherein said memory system is configured to store messages, wherein said memory circuitry comprises a single memory, and wherein said memory architecture is configured to store all of said messages in said single memory.

8. (Original) The method of claim 6, wherein said memory system is configured to store messages, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories.

9. (Withdrawn) A design tool for designing a memory system for implementation using an integrated circuit, comprising:

an input section for specifying attributes of said memory system;

a first database for storing a memory model defining a memory component and a memory interconnection component;

a second database for storing a physical memory configuration associated with said integrated circuit; and

a memory model section, comprising:

a first portion for generating an instance of said memory component and an instance of said memory-interconnection component; and

a second portion for implementing said memory component instance and said memory-interconnection component instance in terms of memory circuitry and interconnection circuitry, respectively, of said physical memory configuration to produce a physical view of said memory system.

10. (Withdrawn) The design tool of claim 9, further comprising:

a third database for storing a set of primitives;

wherein said input section is configured to specify said attributes of said memory system in terms of primitives in said set of primitives.

11. (Withdrawn) The design tool of claim 10, wherein said set of primitives comprises program code for driving said memory model section to produce said logical view.

12. (Withdrawn) The design tool of claim 11, wherein said program code is callable by a second design tool in communication with said input section.

13. (Withdrawn) The design tool of claim 10, wherein said set of primitives comprises descriptions for interpretation by said memory model section to produce said logical view.

14. (Withdrawn) The design tool of claim 9, wherein said memory circuitry is disposed within said integrated circuit.

15. (Withdrawn) The design tool of claim 9, wherein a portion of said memory circuitry is disposed within said integrated circuit, and a remaining portion of said memory circuitry is disposed external to said integrated circuit.

16. (Withdrawn) The design tool of claim 9, wherein said integrated circuit is a programmable logic device.

17. (Currently Amendedl) An apparatus for designing a memory system for implementation using an integrated circuit, comprising:

means for receiving specification data including attributes of said memory system;

~~means for generating a logical description of said memory system in response to said specification data, said logical description defining a memory component and a memory interconnection component; and~~

means for configuring a memory component and a memory interconnection component of a memory model in response to the specification data to generate a

logical view of said memory system; and

means for generating a physical description of said memory system in response to said logical ~~description~~ view, said physical description defining memory circuitry associated with said integrated circuit defined by said memory component, said memory circuitry having an interconnection topology defined by said memory-interconnection component.

18. (Original) The apparatus of claim 17, further comprising:

means for defining said specification data using a set of primitives configured to generate descriptions for said memory system attributes.

19. (Original) The apparatus of claim 17, wherein said memory circuitry is disposed within said integrated circuit.

20. (Original) The apparatus of claim 17, wherein a portion of said memory circuitry is disposed within said integrated circuit, and a remaining portion of said memory circuitry is disposed external to said integrated circuit.

21. (Original) The apparatus of claim 17, wherein said memory component is defined by a memory architecture and a memory interface, and wherein said memory-interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface.

22. (Original) The apparatus of claim 21, wherein said memory system is configured to store messages, wherein said memory circuitry comprises a single memory, and wherein said memory architecture is configured to store all of said messages in said single memory.

23. (Original) The apparatus of claim 21, wherein said memory system is configured to store messages, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories.